



# LOW-POWER CLOCK DISTRIBUTION IN EDGE TRIGGERED FLIP-FLOP

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## ABSTRACT

*The major power consumption in portable electronics devices is due to the long interconnects. These interconnects are global buses, control signals and synchronization clock signals. Other the power dissipation interconnects causes the increase in path propagation delays. The conventional synchronization clocks signals are becoming increasingly difficult for multiple higher frequency integrated circuits because skew, jitter, and variability are often proportional to large latencies.*

*This paper represents gilt edge solution to these problems. This paper's work reduce the sophisticated circuitary by reducing the number of transistors compulsions which further diminishes the stray capacitance. This paper's work reduce the aggressive power with merest feasible area and delay trade off by diminishing transistor size.*

**Keywords – Power Dissipation, Propagation Delay, Higher Frequency, Pass Transistor, Clock Distribution, IOT**

## I. INTRODUCTION

The basic pulse clock cell called as latch is design using series connected CMOS logic with a feedback through PMOS transistor. The data which is to be latch is connected to the “data” input terminal of latch. A NMOS transistor connected to ground terminal is use to reset the latch. When the reset signal is at logic high state, it will turn ON the NMOS and the output is discharge through the NMOS transistor. When the logic level at clock signal is HIGH then the input NMOS transistor turns ON and feed back PMOS transistor turn OFF. The output Q follows the binary at input terminal. Otherwise, when the clock signal is at logic LOW level, then the input NMOS transistor turns OFF and feed back PMOS transistor turn ON. Thus the value at output terminal remains unchanged through feedback PMOS transistor. Fig. 1 shows the schematic logic of pulse latch design on “DSCH” digital schematic simulation tool. This latch requires 6 transistors for design along with one NMOS for reset operation.

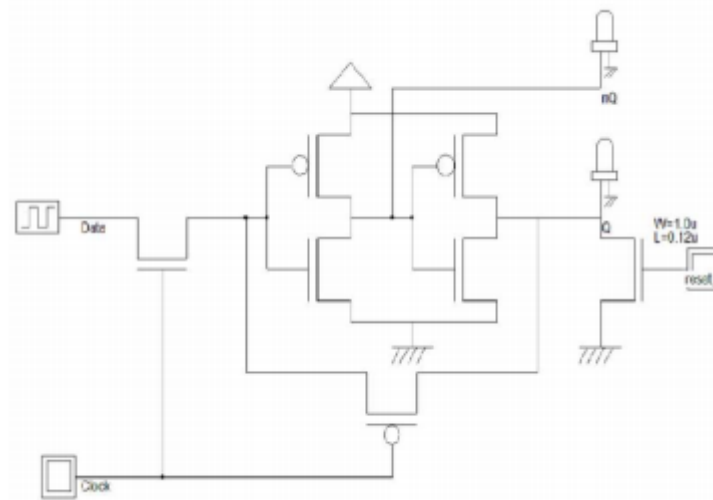


Figure 1: Schematic Design Pulse Latch

## II. RELATED WORK

Work in [1], proposes a new method for clock distribution that uses current, rather than voltage, to distribute a global clock signal with reduced power consumption. While current-mode (CM) signaling has been used in one-to-one signals, this is the first usage in a one-to-many clock distribution network. To accomplish this, they create a new high-performance current-mode pulsed flip-flop with enable (CMPFFE) using 45 nm CMOS technology. Current Mode (CM) signaling schemes perform current-to-voltage conversion and then use the buffered VM clock signal. However, driving the lowest level of a clock distribution network (CDN) with a full-swing voltage results in large dynamic power in addition to significant buffer area to drive the clock pin capacitances [2]. This CM scheme is highly integrated into the FFs that directly receive the CM signal to reduce overall power [3] consumption and silicon area. The proposed CMPFFE is 87% faster, requires similar silicon area and consumes only 7% more power compared to a traditional PFF at 5 GHz. Better yet, the CMPFFE enables a 24% to 62% power reduction on average when used in a CM CDN compared to conventional Voltage Mode (VM) CDN [4].

## III. PROPOSED WORK

### 3.1 Basic Pass Transistor Base Flip Flop

Here we can use negative edge trigger flipflop [5]. The negative edge is the edge where the clock signal changes from 1 to 0. Thus any change in input can affect the output on at this negative edge of clock signal. Flipflops consist of two latches in series as in master slave arrangement controlled by inverted clock signals. During the high level of clock signal the master latch will turn on and slave latch will turn off. The first, called master, changes its state while Clock = 1. The second, called slave, changes its state while Clock = 0. The operation of the circuit is such that when the clock is high, the master tracks the value of the D input signal and the slave does not change.

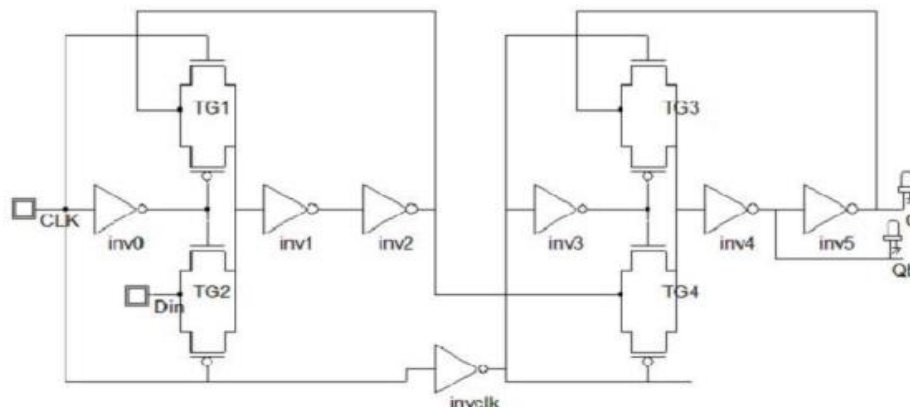


Figure 2: Basic Pass Transistor Base Flip-Flop

### 3.2 Positive Edge Triggered Flip Flop

Another construction of an edge-triggered D flip-flop [5] – [7] uses three SR latches as shown in Fig. 2. Two latches respond to the external D (data) and Clk (clock) inputs. The third latch provides the outputs for the flip-flop. The S and R inputs of the output latch are maintained at the logic-1 level when Clk = 0. This causes the output to remain in its present state. Input D may be equal to 0 or 1. If D = 0 when Clk becomes 1, R changes to 0. This causes the flip-flop to go to the reset state, making Q = 0. If there is a change in the D input while Clk = 1, terminal R remains at 0 because Q is 0. Thus, the flip-flop is locked out and is unresponsive to further changes in the input. When the clock returns to 0, R goes to 1, placing the output latch in the quiescent condition without changing the output. Similarly, if D = 1 when Clk goes from 0 to 1, S changes to 0. This causes the circuit to go to the set state, making Q = 1. Any change in D while Clk = 1 does not affect the output. When the input clock in the positive-edge-triggered flip-flop makes a positive transition, the value of D is transferred to Q. A negative transition of the clock (i.e., from 1 to 0) does not affect the output, nor is the output affected by changes in D when Clk is in the steady logic-1 level or the logic-0 level. Hence, this type of flip-flop responds to the transition from 0 to 1 and nothing else.

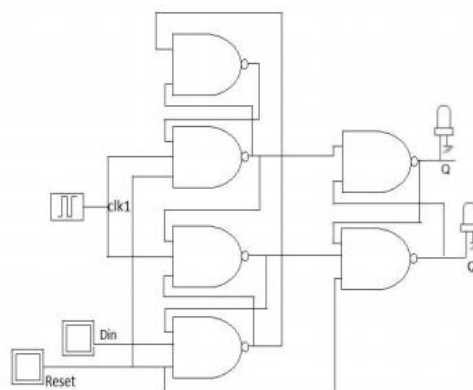
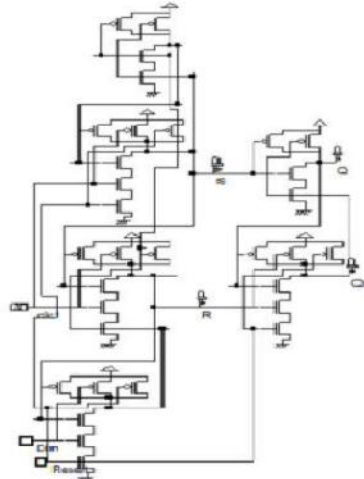


Figure 3: Proposed Cross Connected Positive Edge Triggered D Flip Flop

The CMOS schematic [8] - [9] base edge triggered flip flop is shown in Fig. 3 below. It is a design using two 2 input NAND gate & four 3 input NAND gate with asynchronous reset signal. Here the reset signal is said to be asynchronous because transition on this input will reset the output of flip flop to level '0' without depending on the clock edge. Generally the input is said to be asynchronous [10], as the change in input will affect the output at any instant of time.

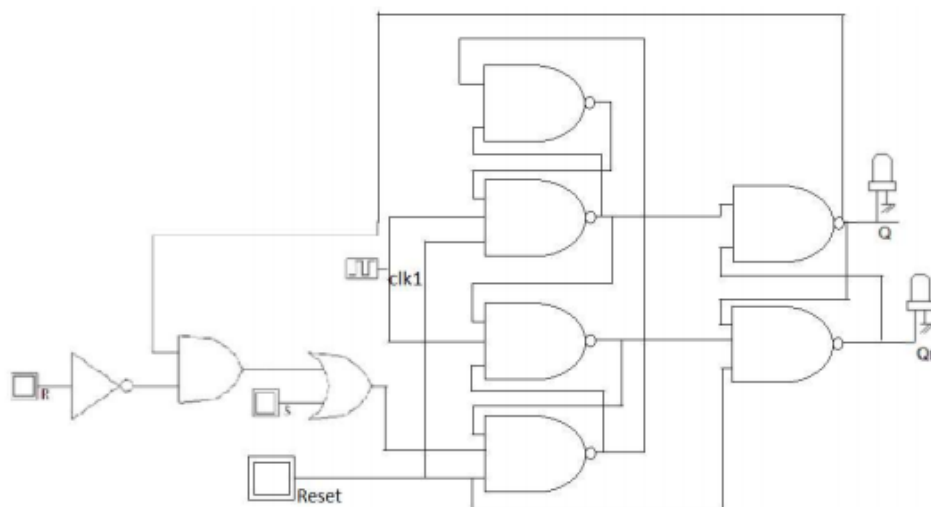


**Figure 4: CMOS Positive Edge triggered Flip Flop Schematic**

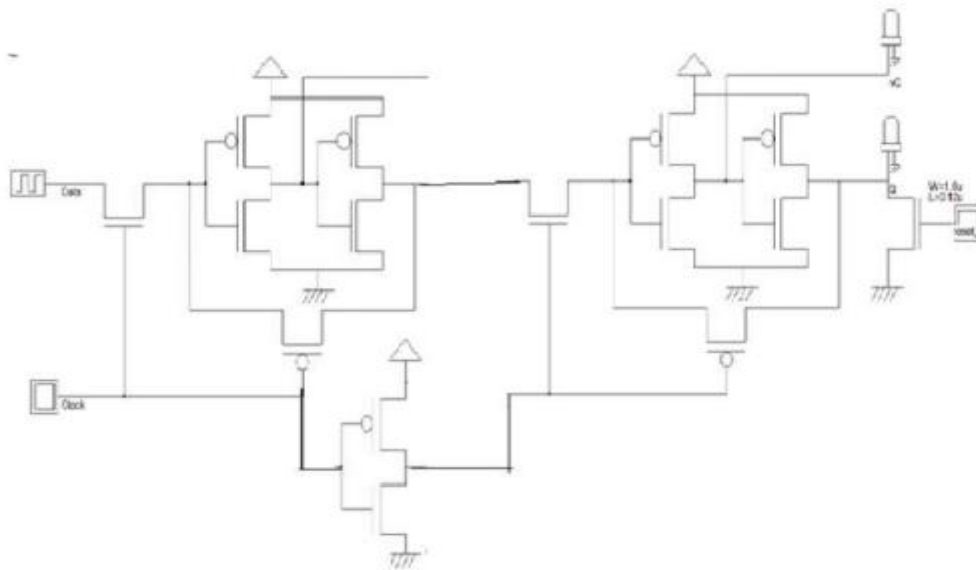
A additional reset input connected to three NAND gates. When the reset input is 0, it forces output Q to stay at 1, which, in turn, clears output Q to 0, thus resetting the flip-flop.

### 3.3 Application Base Other Positive Edge Triggered Flip Flop:

Two other connections from the reset input ensure that the S input of the third SR latch stays at logic 1 while the reset input is at 0, regardless of the values of D and Clk as shown in Fig. 4 below. Fig. 5 represents the transistor realization of SR flip flop.



**Figure 5: Proposed Cross Connected Positive Edge Triggered S R Flip Flop**



**Figure 6: Edge triggered SR Flip Flop using CMOS design**

#### IV. CONCLUSION

This paper discusses the design of edge triggered flip flop with master slave arrangement optimized. Long interconnects causes the increase in power dissipation and path propagation delays. The use of Transmission gate in flip flop design will reduce the number of transistors requirement and also reduces the stray capacitances. This work also reduces the short channel effect by reducing transistor size. This paper presents an optimal solution with a new method which reduces both leakage and dynamic power with minimum possible area and delay trade off.

Since diminishing area of device is a great power of making the latest IOT devices which takes less area to use. This technological work can be used wherever we are restricted to use less power. Power consumption is the weirdest problem of electronic world so this work makes their work efficient and fast.

#### VII. REFERENCES

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