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REVIEW OF DIFFERENT NUMBER OF TRANSISTOR BASED DRAM DESIGN

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ABSTRACT

In modern era characterization of circuit based on reliability, low leakage current less power dissipation and low cost.DRAM provides the advantage of data storage in high density.To optimize the performance of chips,large array of fast DRAM help to boost the system performance. Large array DRAM directly related to higher chip cost. By minimizing the size of DRAM cell, this requirement can be balanced. This paper has comparative study of different number of transistor based DRAM design and its power analysis which is based on various tools and technology.

Keywords— DRAM, Power dissipation, leakage current, fin FFT, Self voltage level.

I. INTRODUCTION

DRAM is generally produced in large volumes. It can store data in high density. Memory cells are identified by address. To ensure the correct memory operation a careful timing of read –write RAM can be classified as (1)Access (2)read-write (3) input-output. A clock signal appears at the input of memory module(decoder).Decoder selects a single word line.After decoding sensing procedure performs by sens–amplifier. DRAM is volatile memory means when power is turned off, data loses. In this memory each bit of data stored in a separate capacitorwithin an IC. The charging or discharging of capacitor represent two values of bit called ‘1’ or ‘0’. Because of this periodically refreshing this memory is Dynamic.Random access means any data from the memory can directly access by PC processor.

II. WORK HISTORY

In this paper has the comparative study of already designed dram, based on different no of transistor like1- T DRAM, 3-T DRAM, 4-TDRAM,3-T DRAM using Fin FFT using various tools at specific technology.

Information inside of DRAM stored in binary form(‘0’,’1’)by the capacitor and this storage element access by the transistor. As the main memory in computer DRAM is widely used.There is capacitor is a main storage device therefore DRAM cell to be realized in a much smaller silicon area compared to SRAM.

III. DRAM CELL USING 1-TRANSISTOR

Capacitor is manufactured separately in each storage cell. Enabled the word line, the written operation performed by placing either ‘1’ or ‘0’ charge into the storage capacitor. The read operation is damage.

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This process has done during a write cycle by openingthe cell transistor(gate to Vcc)and presenting either Vcc or 0 V(Gnd) at the capacitor .The word lineof transistor is then held at ground to isolate the capacitor charge[1].If the stored charge of capacitor is changed with bit line, its charge can be damaged. Since the capacitance of the storage cell is smaller than that of the bit line by at least about 10 times,only a small voltage difference is produced at the

bit line depending on the data of the storage cell. Therefore an amplifier to sense the signal difference and rewrite the data into the cell is required for the successful read operation[2].

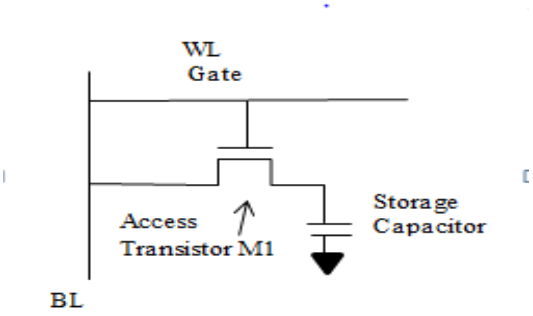

Figure 1.One transistor DRAM cell.

Sensing means the detection and determination of data content of selected memory cell [2]. Sensing shall be non-destructive or destructive and is widely dependent on open or close book architecture in which the CMOS memory is being laid out. The data content of the selected memory cell may be altered or unchanged.SRAMs, ROMs, PROMs etc uses non-destructive sensing and Dynamic RAMs uses destructive sensing.

Sensing circuits generally comprises of sense amplifiers, precharge, reference and load circuits, bitlinedecoupler, an accessed memory cell and other necessary memory control circuits.The control circuits and parasitic elements coupled to horizontal and vertical bit lines generate combined impedance which significantly effects the operation of random access memories.

IV. POWER DISSIPATION USING 3-T AND 4-T DRAM CELL

In the analysis of power dissipation in DRAM celldesign for nanoscale memory result shows that power consumption will increasesif the width of transistor increases,they use the tanner tool for 3-Transistor and 4-Transistor DRAM.

Channel Width	3T-DRAM Power Consumption	4T-DRAM Power Consumption
90 nm	$4.19*10^{-5}$mw	0.923mw
0.3 µm	$6.481*10^{-5}$mw	0.95mw

Table1.Comparison of power consumption with channel width.

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Another 3-T DRAM with self-controllable voltage level to reduce low leakage current[3].They used 0.21µm technology, the simulation is done by Microwind 3.1 tool. In this design two inverters one at upper part and one in lower part used, then the leakage current reduces upto 57%.In another literature work has design of nanoscale 3-T DRAM using Fin FET thiswork preferred 32nm technology by HSPICE Too[4l. The layout of operation mode of Fin FET is similar to traditional FET (source, gate and drain terminal). In MOSFET the channel between source and drain is built as a three dimensional bar on top of the silicon substrate that is called fin.The gate electrode is then wrapped around the channel, so that there can be several gate electrodes on each side which leads to reduced leakage effects and enhanced drive current. In FIN technology various parameters will also be changes like channel doping, gate work function, body thickness etc.

V. CONCLUSION

This is the review paper based on various research of DRAM design based on the number of transistor, there are focused on power dissipation ,low leakage current by using different designing tools and technology.

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