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DESIGN AND SIMULATION OF 12T SRAM CELL USING TRANSMISSION GATE AS ACCESS TRANSISTOR ON 45 nm TECHNOLOGY

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ABSTRACT

Technology is contracting down rapidly and almost all the low power gadgets require memory which works faster, considering that new high speed SRAM cell has been designed. The designed 12T SRAM cells also consume less power. In our design, transmission gates have been used as access transistors. The Simulation results such as power dissipation, delay, PDP (Power Delay Product) of the proposed SRAM cell have been calculated and contrasted with those of some other existing models of SRAM cell. The proposed configuration gives 61% diminishment in power dissipation. For design and simulation purpose, Tanner EDA Tool V.14.1 at 45nm CMOS has been used.

Keywords:Transmission Gate,Low power Dissipation, Static noise margin, SRAM Swing voltage,Tanner tool.

I. INTRODUCTION

Decrease in channel length demands an circuit which consume less powerand lessdelay. High speed portable device such as mobile,laptop, CPU demands high speed memory which consume less power and gives high signal to noise margin. ram memory is very important part of any storage circuitry. Dynamic power dissipation and leakage current are the main issues of high speed SRAM cells because this unwanted power dissipation reduces the battery backup life of portable devices. So it is required to have a SRAM cell design, having both low static and dynamic power dissipations.

In this present work a novel low power 12T SRAM cell is proposed. A charge recycling technique is used to minimize the leakage currents and static power dissipation during the mode transitions. Two voltage sources are used at the output nodes to reduce the swing voltages, resulting in reduction of dynamic power dissipation during switching activity. The different performance parameters have been determined for the proposed SRAM cell and compared with those of the other existing SRAM cells.

The paper is organized as follows: Section 2 discusses about some existing SRAM cells, Section 3 describes circuit design and working principle of the proposed novel 12T SRAM cell. Section 4 describes the detailed analysis of the characteristics of the proposed cell and comparison with other existing SRAM cells and finally, Section 5 concludes the paper.

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II. 12T SRAM cell

In order to overcome the problem associated with conventional SRAM cells and other existing SRAM cells, the authors proposes a multi threshold complementary metal oxide semiconductor (MTCMOS) based 12T SRAM architecture to achieve low static and dynamic power dissipations for read and write operations and better stability. In the proposed design two voltage sources V1 and V2 are connected to the outputs of the bit line (BL) and bitbar line respectively. Two NMOS transistors VT1 and VT2 are used, one connected with the BL and the other with the BL directly to switch ON and switch OFF the voltage sources during write operations. The voltage sources reduce the swing voltage during write '0' and write '1' operation at higher frequencies. This reduction in swing voltage reduces the dynamic power dissipation. The two high threshold voltage (HVT) sleep transistors S1 and S2 are used. NMOS sleep transistor S1 connects node M (also called virtual groundnode) to ground whereas the PMOS sleep transistor S2, connects node N (also called the virtual supply node) to Vdd supply.The low threshold voltage (LVT) transmission gate (TG) is connected between the two virtual nodes M and N for providingcharge sharing. The proposed design is illustrated Sleep transistor control signal (ST) and charge sharing controlsignal (CS) provide the switching activity control on sleep transistors and transmission gate, respectively. Sleep transistorsdisconnect logic

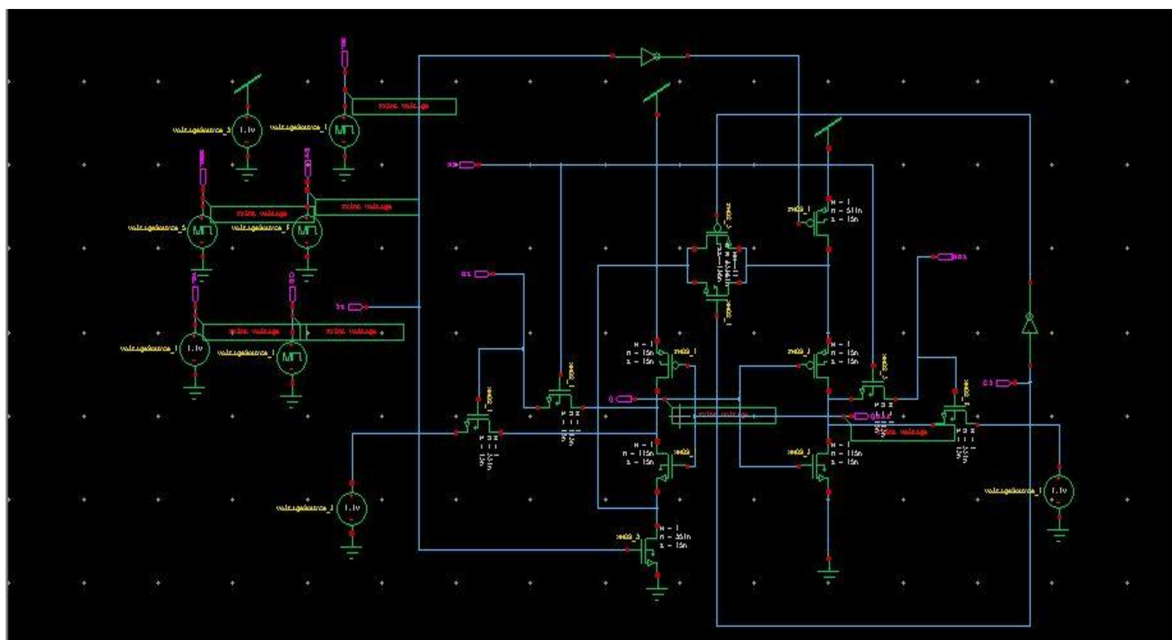

Fig.1The 12T SRAM cell.

cells from the supply and/or ground. Charge recycling technique reduces the leakage current while transistorsflip its mode from active to sleep and sleep to active. Reduction of leakage current reduces the static power dissipation.

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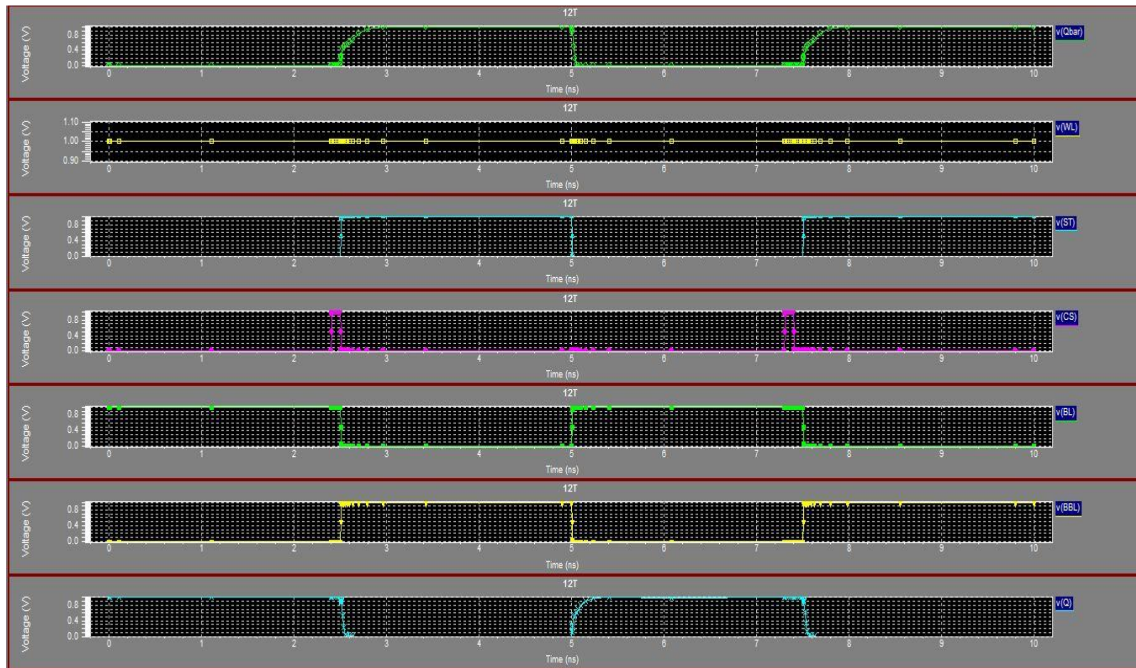

Fig.2 Simulation Diagram of the 12T SRAM cell.

III. PROPOSED 12T SRAM CELL

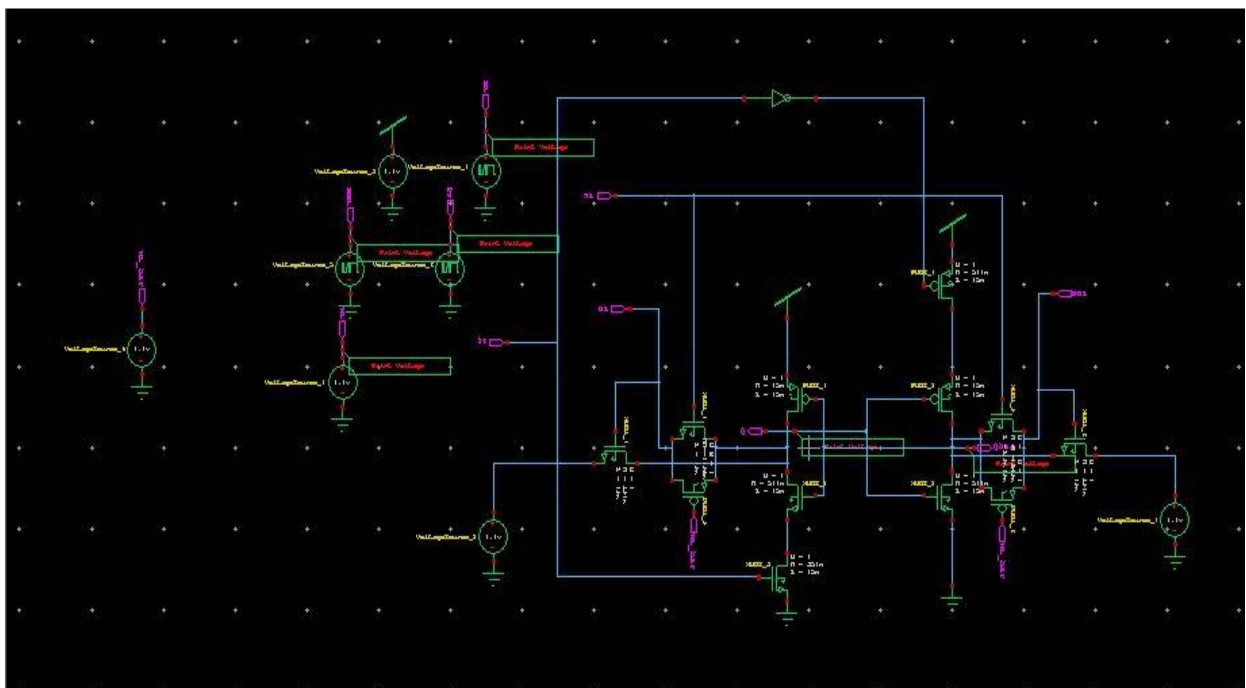

Fig.3 The proposed 12T SRAM cell.

Fig.3 shows circuit diagram of new proposed 12T SRAM cell working of proposed design is same as that of previous 12TSRAM cell but here we made some modification such as, In modification, what we have done is We have removed the charge sharing block i.e. TG(Transmission Gate) structure and inverter used, so number of transistors reduced.We have placed TG in place of NMOS of both the access transistors, this will ensure true

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levels of output as we already know the advantage of TG over MOS. And we can see the effect of these modifications in our results, which are in next section.

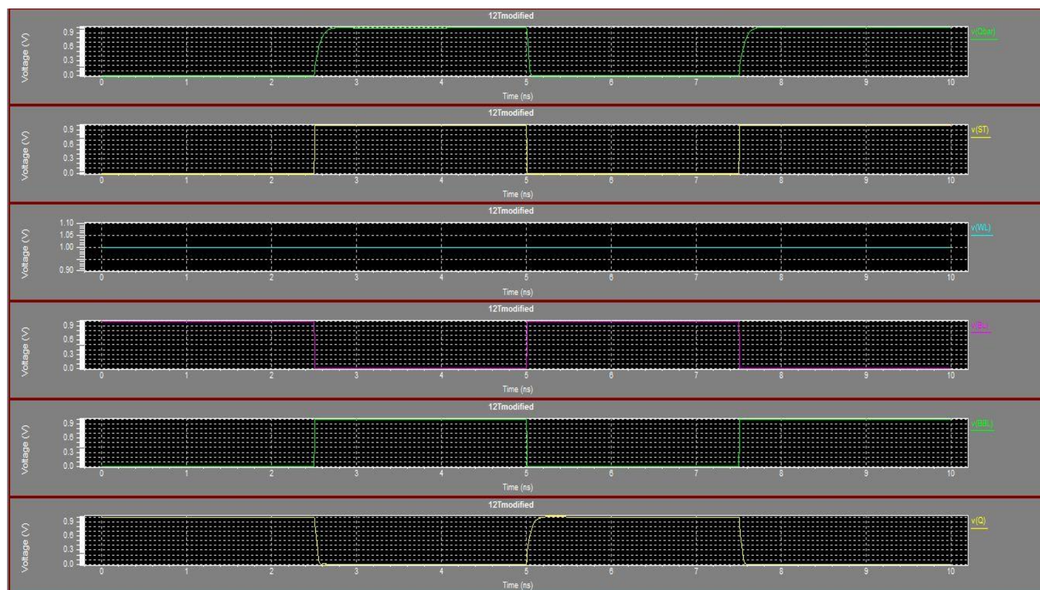

Fig.4Simulation Diagram of the proposed 12T SRAM cell.

IV. RESULT

A proposed design is simulated using Tannet EDA Tool using TSMC 45nm technology at 1V supply.fig.4 shows output waveform of proposed 12TSRAM cell. Obtained result of new design is compared with old 12T SRAM cell and tabulated in table 1 as shown.

Designs	Power	Write 0		Write 1	
		Delay	PDP	Delay	PDP
12T SRAM	1.9844 uw	21.054 ps	41.780 aJ	22.995 ps	45.632 aj
Proposed 12T SRAM	0.8000 uW	24.227 ps	19.384 aJ	20.921 ps	16.738 aj

Table 1. 12T SRAM vs proposed 12T SRAM cell Comparison

V. CONCLUSION

As, technology changes day by day power dissipation and stability are major issue of any high speed device. The proposed SRAM cell is solution of this problem which uses transmission gate as access transistor to give less power dissipation with high speed operation. A proposed novel 12T SRAM cell gives high signal to noise margin than previous design. Such high speed ,high SNM, SRAM cell can be used in memory architecture such as flash memory. Simulation is carried using Tanner Tool on TSMC 45nm technology.

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